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A DIRECT-READING FOUR-DECADE DIVIDER

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Special Research Branch
Radio Division III

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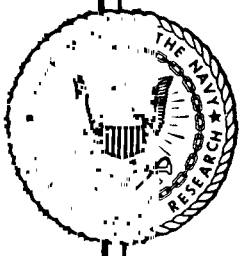

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ABSTRACT

A direct-reading four-decade frequency divider, successfully completed at NRL, is an improvement over other frequency dividers since it provides accurate and exact division by any whole number from 1 to 10,999, including prime numbers. The integer may be chosen at will from four ten-position selector switches that are directly calibrated for division ratio in decade fashion. The divider operates for any input frequency from the low audio range up to 450 kc without any form of adjustment except the selection of division ratio. This equipment was developed to provide step-frequency control of a disciplined oscillator as used in a frequency meter.

PROBLEM STATUS

This is a final report on one of the three major phases of the frequency-meter problem; work continues on the other two phases.

AUTHORIZATION

NRL Problem R10-49
RDB Project NR 510-490

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A DIRECT-READING FOUR-DECADE DIVIDER

INTRODUCTION

A proposal for a direct-reading frequency meter was made in NRL Report 3527 entitled "Portable Precision Frequency Meter." The most unique but least known feature in the recommendation was the direct-reading four-decade divider which would provide division by any integer, including prime numbers up to 10,999, without becoming frequency sensitive below its upper operating limit. Work on the frequency meter was logically begun on this,the most difficult component. Since that time, a working model of a two-decade divider was developed, constructed, and demonstrated to prove the principle of its operation. Emphasis was then placed upon other phases of the frequency-meter problem. Recently, a phase of this problem which required the four-decade divider was reached; such a unit has now been completed in final laboratory form, and this report records the satisfactorily completed development.

The divider differs from other types of multiple-decade dividers because division by any whole number, including prime numbers, may be selected and continuously obtained, and the actual division ratio may be directly read from the dial settings. For example, two simple decade dividers, each capable of being set to divide a frequency by any whole number between one and ten, would when cascaded be unable to divide that frequency by prime numbers above ten or by numbers with factors above ten (such as 11, 13, 17, 19, 22, etc.,to 99). In most cases such dividers are not direct reading. However, by selection of direct-reading decade controls, the four-decade divider described in this report will provide division by all whole numbers including these prime integers. A combination of four decades enables division by all whole numbers from one to 10,999. The present upper frequency limit of the four-decade divider, approximately 450 kc, is adequate for its intended application.

PRINCIPLE OF DIVISION

The divider (Figure 1) may be operated with 1, 2, 3, or 4 decades, but an explanation of the two-decade divider combination will show most of the current arrangements. A bottom view of the units chassis is shown in Figure 2, and the thousands chassis is presented in Figure 3 to show the wiring arrangement. In a two-decade system, each decade contains four bi-stable binary-type dividers in cascade. These consist of a double triode connected so that one triode will conduct while the other is cut off, and a stable state will exist for conduction by either triode. If a negative indication is used for plate polarity when the tube is conducting and a positive indication is employed when the tube is non-conducting, a table of polarities may be determined for each plate of the four binary dividers for any number of input pulses. This divider uses triple coincidence of positive

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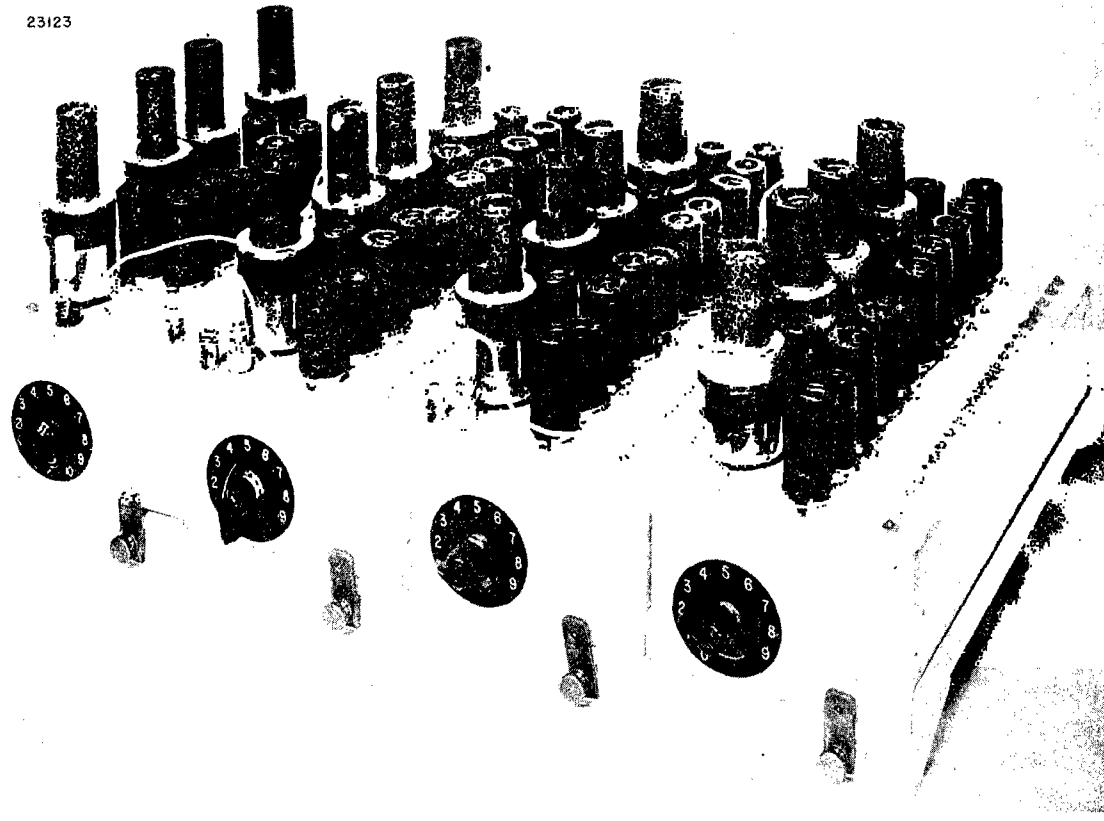

Figure 1 - Four-decade divider

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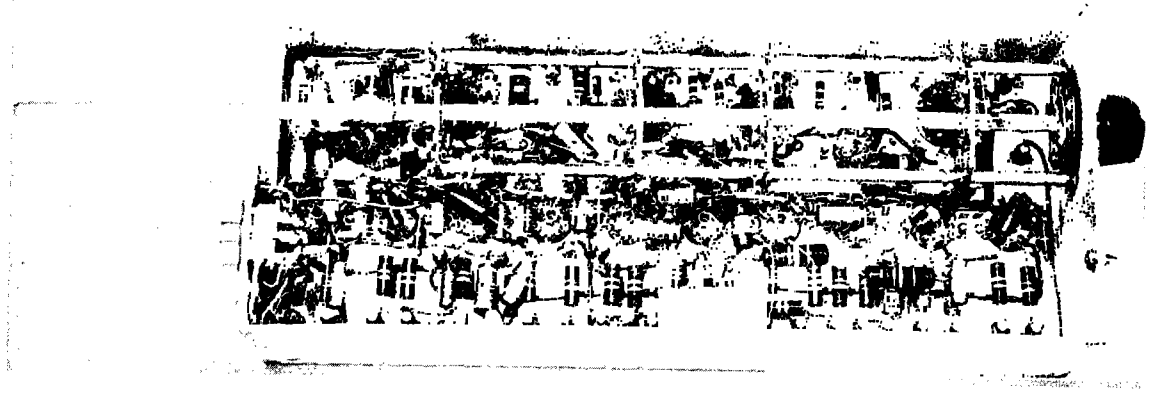

Figure 2 - Units-decade chassis bottom

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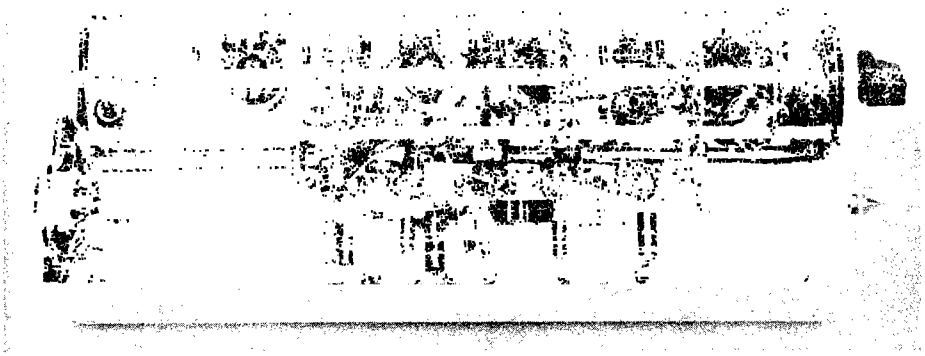


Figure 3 - Thousands-decade chassis bottom

signals derived from the binaries to cause reset of the binaries to a known starting polarity at a selected count; the reset pulse will then occur at the desired division. Division is accomplished by counting the number of units digits (as indicated by the selected division ratio) in a triple-coincidence mixer, which will now be called the variable mixer. Thereafter, this mixer will be disabled and the decade will then count by ten in a second triple-coincidence mixer, which will be designated the fixed mixer. Although both mixers are required in the input decade, only the variable mixer is necessary in the output decade. A pulse signal is fed from the input to the output decade after each group of ten input signals. The output decade counts the number of these as indicated by the tens digit of the division ratio and then resets the variable-mixer circuit of the input decade. Other decades, used as in a four-decade divider, each contain both variable and fixed mixers. Tables 1 and 2 show the reset or reference polarities and the resulting polarities at subsequent input cycles for the output and input decades, respectively. A different reference polarity was chosen for both input and output decades. It will be observed from Table 1 that three positive binary plates may be chosen for any given count between one and ten which have not previously been positive at the same time. A selection was made for each count of one through ten for both types of decades, and the selected plates are encircled in Tables 1 and 2. Where the encircled plate is negative, amplifier inversion will produce a positive polarity at the triple-coincidence mixer. Coupling between binary plates and each input of the mixer is made through a selector switch so that selection of plates, and hence division ratio, may be made from the front panel of the decade. In the input-type decade, one of the mixers is used only for division by ten and therefore the inputs are permanently connected. This selection is shown in Table 2 where squares enclose the selected plates.

Division by Numbers 10 through 110

In a two-decade divider combination (Figure 4), there are essentially two different counting procedures which involve different reset loops. The first procedure applies for selection of division by ratios of 10 through 110, and the second applies for counts of one through nine.

Here the means of dividing is accomplished by first setting the wafers of the rotary selector switch of each decade for the desired division ratio. Coincidence at the input-decade variable mixer will occur when the selected number of units counts has been reached. The mixer output resulting from coincidence will reset the binary dividers to the initial starting polarity through a reset loop consisting of the mixer, gate, one-shot multivibrator, delay amplifier, unidirectional coupler, binary reset amplifier, and

TABLE 1
Binary Plate Polarity for Thousands Decade*

No. of Input Pulses	P_1 P_2	P_3 P_4	P_5 P_6	P_7 P_8
0 (Reset Ref.)	+ -	+ -	+ -	+ -
1	⊖+	⊕-	⊕-	+ -
2	+⊖	-⊕	⊕-	+ -
3	⊖+	-⊕	⊕-	+ -
4	+⊖	⊕-	-⊕	+ -
5	⊖+	⊕-	-⊕	+ -
6	+⊖	-⊕	-⊕	+ -
7	⊖+	-⊕	-⊕	+ -
8	+⊖	⊕-	+ -	-⊕
9	⊖+	⊕-	+ -	-⊕
10	+⊖	-⊕	+ -	-⊕

* Encircled polarities indicate plates utilized at corresponding number of input pulses.

TABLE 2
Binary Plate Polarity for
Units, Tens, and Hundreds Decades*

No. of Input Pulses	P_1 P_2	P_3 P_4	P_5 P_6	P_7 P_8
0 (Reset Ref.)	- +	- +	+ -	- +
1	+⊖	+⊖	-⊕	- +
2	⊖+	+⊖	-⊕	- +
3	+⊖	⊖+	-⊕	- +
4	⊖+	⊖+	-⊕	- +
5	+⊖	+⊖	+ -	⊕-
6	⊖+	+⊖	+ -	⊕-
7	+⊖	⊖+	+ -	⊕-
8	⊖+	⊖+	+ -	⊕-
9	+⊖	+ -	⊖+	⊕-
10	⊡+	+ -	⊡+	⊞-

* Encircled polarities indicate plates utilized at corresponding number of input pulses.

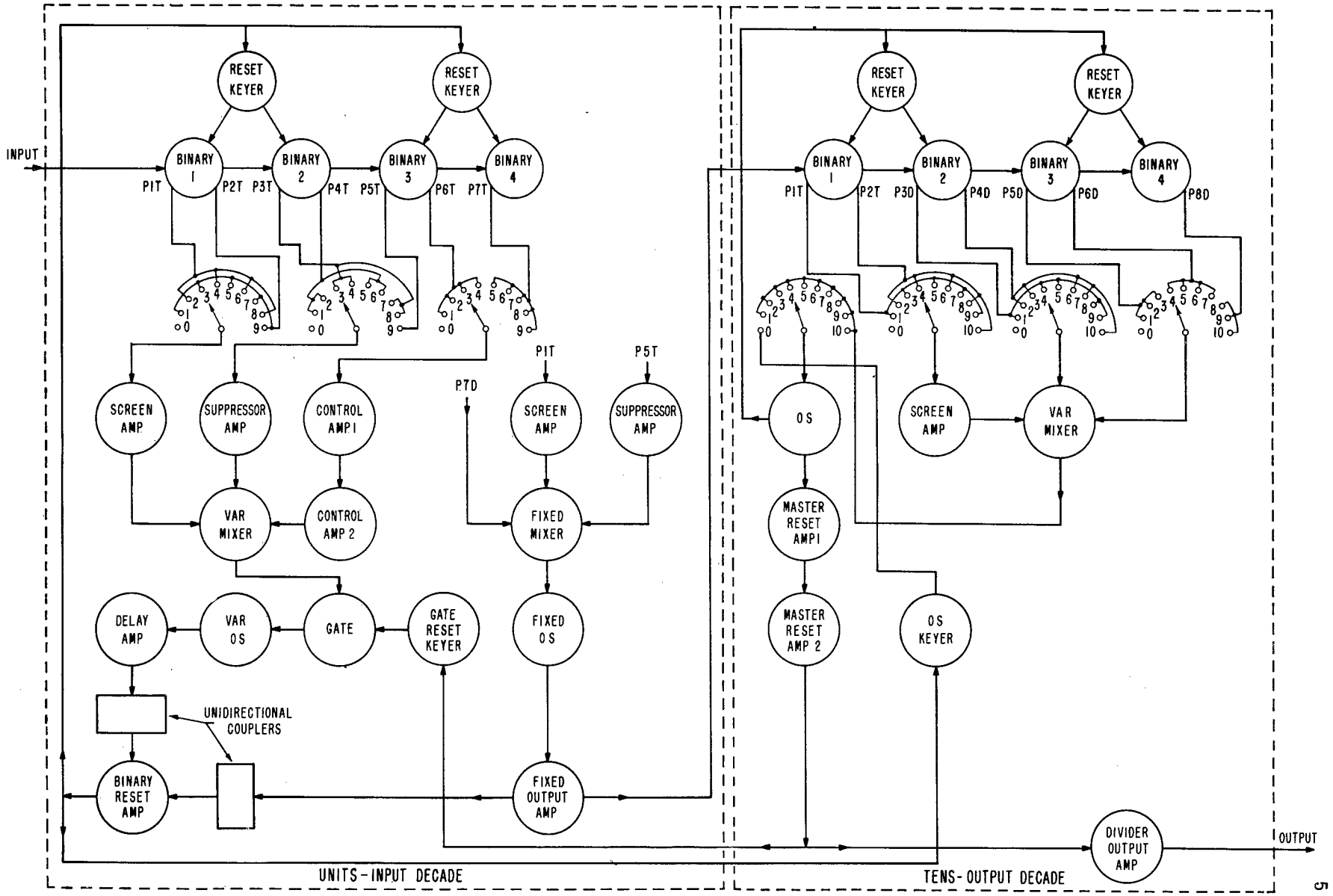


Figure 4 - Block diagram of direct-reading two-decade divider

binary reset keyer tubes. This will be called reset loop No. 1. In the reset process the gate is disabled, and when the units count again occurs, no signal will pass through loop No. 1 to reset the binaries; hence they will continue until the tenth pulse following reset by loop No. 1. Coincidence then occurs in the fixed mixer which provides an output that (a) resets the units binaries through reset loop No. 2, consisting of fixed mixer, fixed one-shot multivibrator, output amplifier, unidirectional coupler, binary reset amplifier, and binary reset keyers and (b) provides an output signal that is fed to the input of the next decade. The first output pulse, therefore, occurs from the units decade after the selected units count plus ten additional pulses have been made. Thereafter, the units decade continues to provide one output pulse for every ten input pulses, and the units binaries are reset after each group of ten through loop No. 2 until a master reset signal is derived from the second decade.

The wafer-switch selection of the output decade determines the number of input pulses at which coincidence occurs in the single mixer of this decade. At coincidence, the binaries of this decade are reset through loop No. 3 which consists of the mixer, one-shot multivibrator, and binary reset keyers. Simultaneously, the one-shot-multivibrator output is utilized to reset the units-decade gate through the master reset loop (No. 4) which contains master reset amplifier No. 1, master reset amplifier No. 2, and the gate reset keyer of the input decade. This action, occurring at the completion of the selected count, returns the gate to the initial starting condition. The two-decade divider will continuously repeat the preceding cycle of operation to provide continuous division by the selected division ratio.

For example, if a division ratio of 43 is selected, the units-decade variable mixer will provide an output pulse at the third input cycle, the gate will be disabled, and the units-decade binaries are reset through loop No. 1. After ten more input pulses, which will now total 13, the fixed mixer will provide an output and reset the units binaries through loop No. 2. The fixed-mixer output occurs thereafter for each group of ten input pulses with the units binaries reset via loop No. 2 after each until the third group of ten. Since one output pulse was obtained for 13 input pulses and one after each of three additional groups of ten, coincidence then occurs in the second decade (set to four), the second decade binaries are reset through loop No. 3, and the units gate is reset by loop No. 4 to complete the cycle of operation. Both decades are now in the initial starting polarity and will repeat the preceding cycle to continuously divide by 43.

Division by Numbers of 1 through 9

An additional wafer switch in the output decade is required for division by numbers less than ten. The units decade operates in the predescribed manner, and coincidence occurs in the variable mixer at the selected count. The resulting signal, however, not only resets the binaries through loop No. 1 but also provides a signal through loop No. 5 and the added output-decade wafer switch to trigger the master reset one-shot multivibrator of the output decade. This action initiates the reset of the units-decade gate through loop No. 4 prior to the next input pulse. Loop No. 5 consists of the gate, variable one-shot multivibrator, delay amplifier, binary reset amplifier, one-shot keyer (output decade), and returns to the units gate via loop No. 4. Since master reset occurs before the next input pulse, the gate will always provide the output and never permit coincidence to occur in the fixed-mixer circuit. Hence for division by numbers below ten, no input is presented to the binaries of the output decade, and therefore they are not used.

TIME CONSIDERATIONS IN THE DESIGN OF THE MULTIPLE-DECADE DIVIDER

Input Circuit

The use of the four-decade divider as now proposed for the frequency meter requires operation over an input frequency range of about 30 to 370 kc. Tests have shown satisfactory binary operation over a much wider range, provided that the input signal is shaped into a negative pulse of sufficiently fast fall time, has an amplitude above the required minimum, and has less than the maximum permissible width. Time constants in the binaries have been minimized to provide high-frequency operation. These short time-constant circuits, however, will not pass low frequencies in amplitudes sufficient for binary keying unless the low frequency is converted into a pulse which contains the required high-frequency component. For the binaries used in this divider, the pulse fall time should be 0.4 microsecond or less. At very low frequencies, a large amount of gain is required to provide the required negative input-pulse fall time while at the higher frequencies little or no gain is required. There is no low input-frequency limit, provided the required fall time is supplied. The desired input-pulse amplitude is in excess of 50 peak volts, but this is not a critical value. As far as binary operation is concerned, the upper frequency determines the maximum allowable width of the input pulse, and this width obviously must be somewhat less than the time between input cycles at the upper operating frequency. A more stringent requirement, however, is imposed for operation of the binaries in conjunction with the reset circuits. If the input pulsewidth is greater than the time delay in loop No. 1 (Figure 5), the input keying signal and the binary reset signal may attempt to simultaneously trigger the binaries in opposite directions and pulse bucking will result in erratic operation. To use the divider in the frequency meter, the maximum allowable input pulsewidth has been determined to be less than 0.6 microsecond.

Figure 6 is a schematic diagram of the pulse shaper that has been successfully used with the dividers described in this report. The gain is sufficient to provide a satisfactory 0.4-microsecond fall time for sine-wave input frequencies as low as 1000 cps. The output pulsewidth is approximately 0.4 microsecond and the fall time is less than half this value.

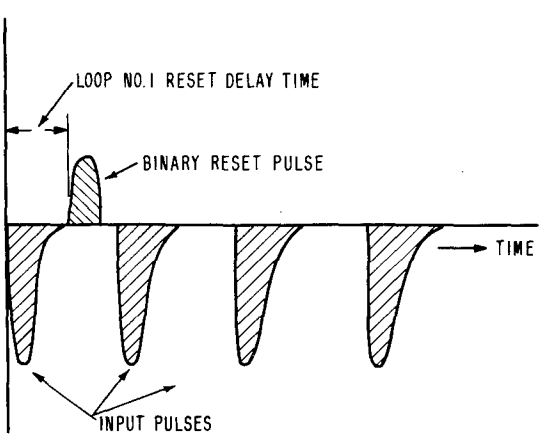


Figure 5 - Time sequence of input and reset pulses

Loop No. 1

Time considerations and pulse requirements (those of the units and thousands decades, respectively) of this and other reset loops may be described with reference to the schematic diagrams of Figures 7 and 8 as well as reference to the block diagram of Figure 4.

The signals to the three grids of the variable mixer in the input-type decade must be shaped and amplified for best divider operation. At the mixer grids, the time of the rise and fall must be rapid or a change in the mixer-grid bias voltage will change the exact time at which coincidence occurs and the binary-reset delay time for loop No. 1. The screen grid requires more driving power than the other grids of the 6AS6 mixer tube, but the average power may be minimized by operating the screen grid from the narrowest pulsewidth signal. The output of the first wafer switch has been differentiated and it is the narrowest of the coincident pulses; hence the output of the first wafer was chosen to feed the screen grid. It would be extremely difficult to maintain the positive screen-grid signal with ac coupling for the times produced at the second and third wafer switches.

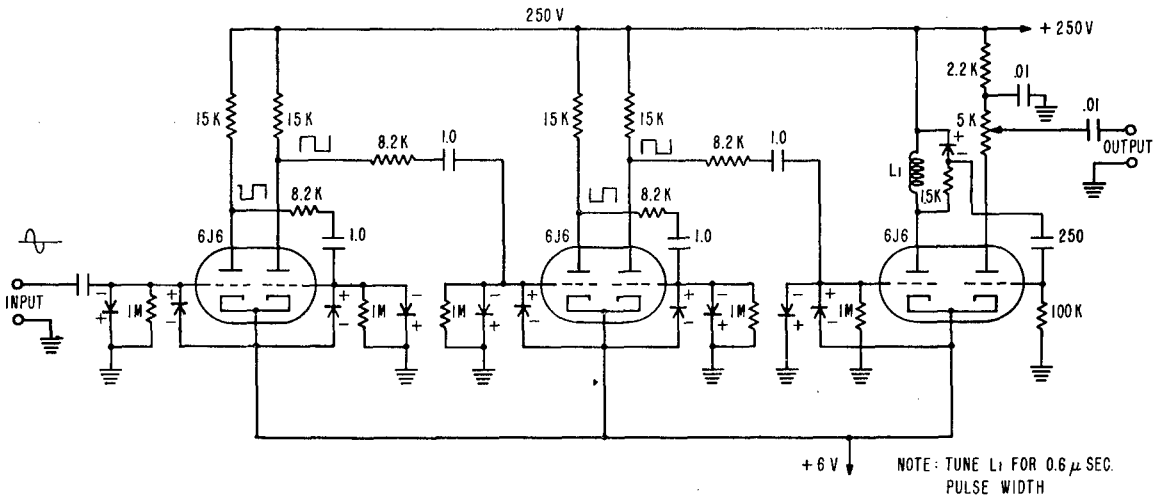
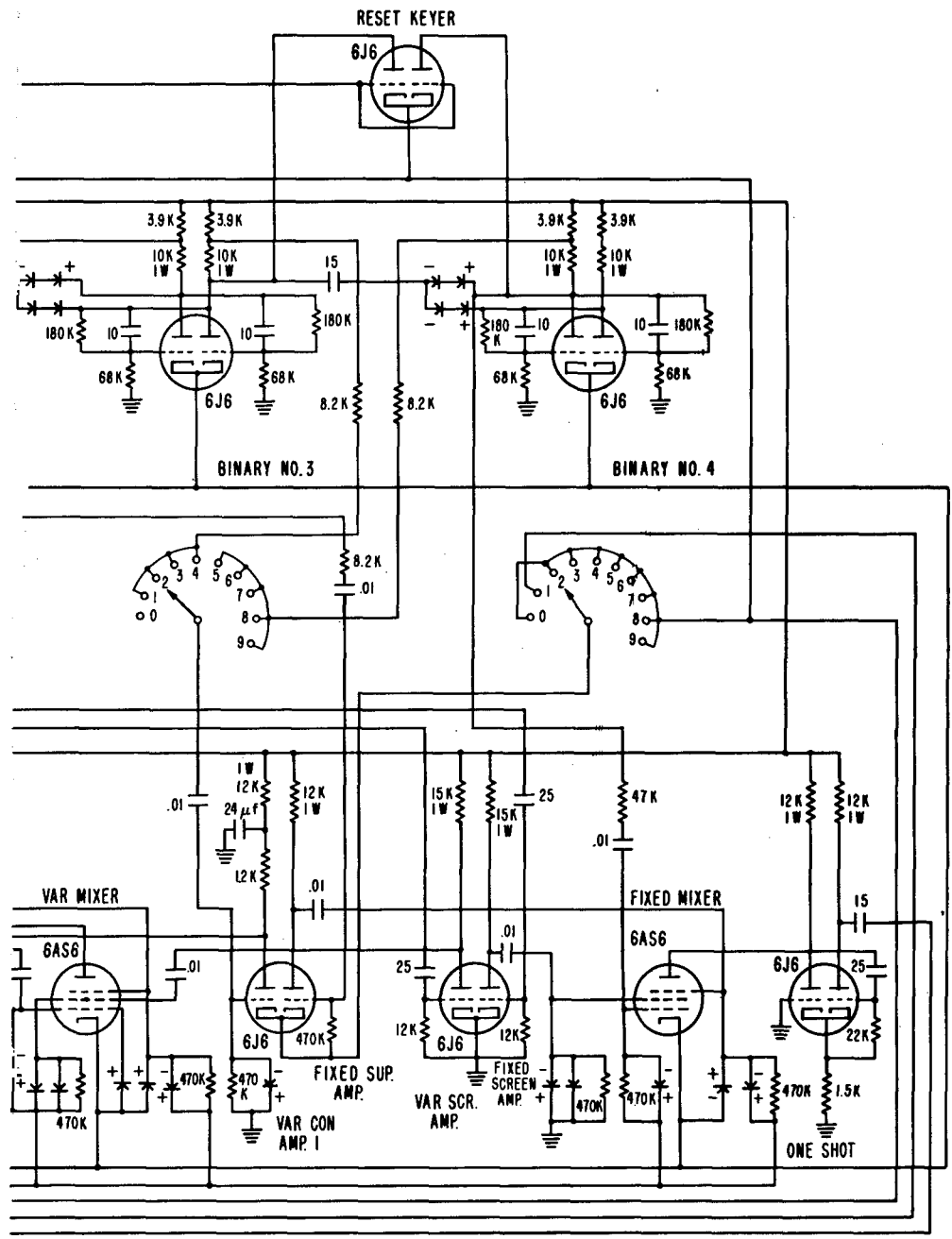


Figure 6 - Schematic diagram of input pulse shaper

The suppressor grid amplifier was designed to reduce delay of the mixer-signal rise and fall as much as possible. The use of the amplifier permits the input signal to be obtained from a tap on the binary-plate load resistor, thereby reducing the capacitive load on the direct binary plate.

Two amplifiers were used to couple the binary signals to the mixer control grid and permit the use of the positive binary signal to cause coincidence at the mixer without excessive binary loading. The use of a single amplifier was attempted but proved unsatisfactory. The single amplifier was zero biased, but it was not convenient to insert delay in this type amplifier although use of a crystal-diode gate type of delay was attempted with limited success. A delay circuit is required between the third wafer and the mixer control grid, especially if a single amplifier stage is used. The signal at the binary plate has the relatively long rise time of 1.2 microseconds compared to the fall time of 0.4 microsecond. Unless delay is added in the control grid circuit, the resulting division ratio will erroneously be 1, 5, and 5, respectively, on count selections of 3, 7, and 9. The difficulty results from the fact that the long rise time of the second wafer output although amplified is still relatively slow in cutting off the suppressor grid. In the meantime, the fast fall time of the third wafer output when amplified becomes still better and brings the mixer control grid into conduction before the suppressor grid is cut off. Use of a double amplifier eliminates this difficulty by utilizing the positive binary signal that has the slower rise time to drive the mixer control grid positive and by using the first amplifier, which is normally nonconducting, as a means of inserting a delay. Reference to Table 2 will show that this inserted delay will add directly to the reset time of loop No. 1 and reduce high-frequency response only when counts 1 or 5 are selected. For this reason the delay is minimized in positions 1 and 5 by reducing the delay-circuit bias voltage which is normally obtained from a fourth wafer switch in the units-type decade. Delay is not required for counts 1 and 5.

The principle of the delay-circuit operation is to provide crystal-diode gating with freedom of swing within the gate in excess of the cutoff value of the first-amplifier control grid (Figure 9). The amplifier is normally biased beyond cutoff, and the grid is allowed to swing only by the magnitude of the gate width. An increase or decrease in the gate width, however, is accompanied by a corresponding increase or decrease in the delay. A 0.4-microsecond delay was found most satisfactory for counts 3, 7, and 9 on which the delay is primarily required.



!-0.6 WIDE-0.2 FALL)
ESET INPUT
'SS OUTPUT
PUT

units decade

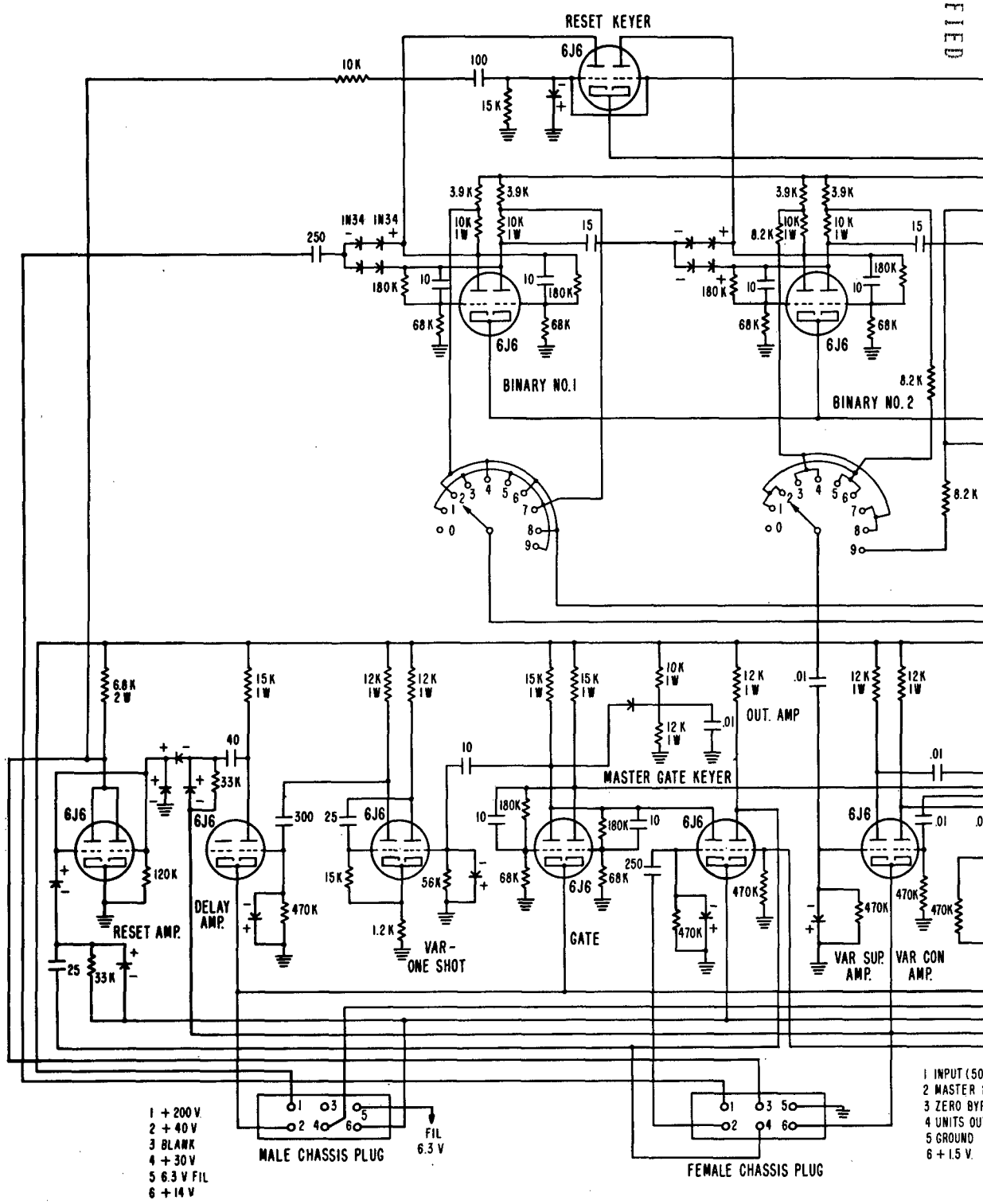
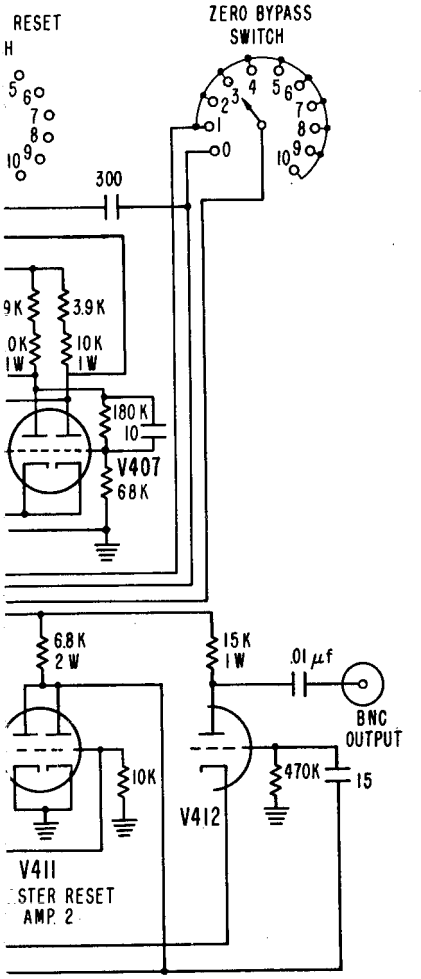


Figure 7 - Schematic diagram of



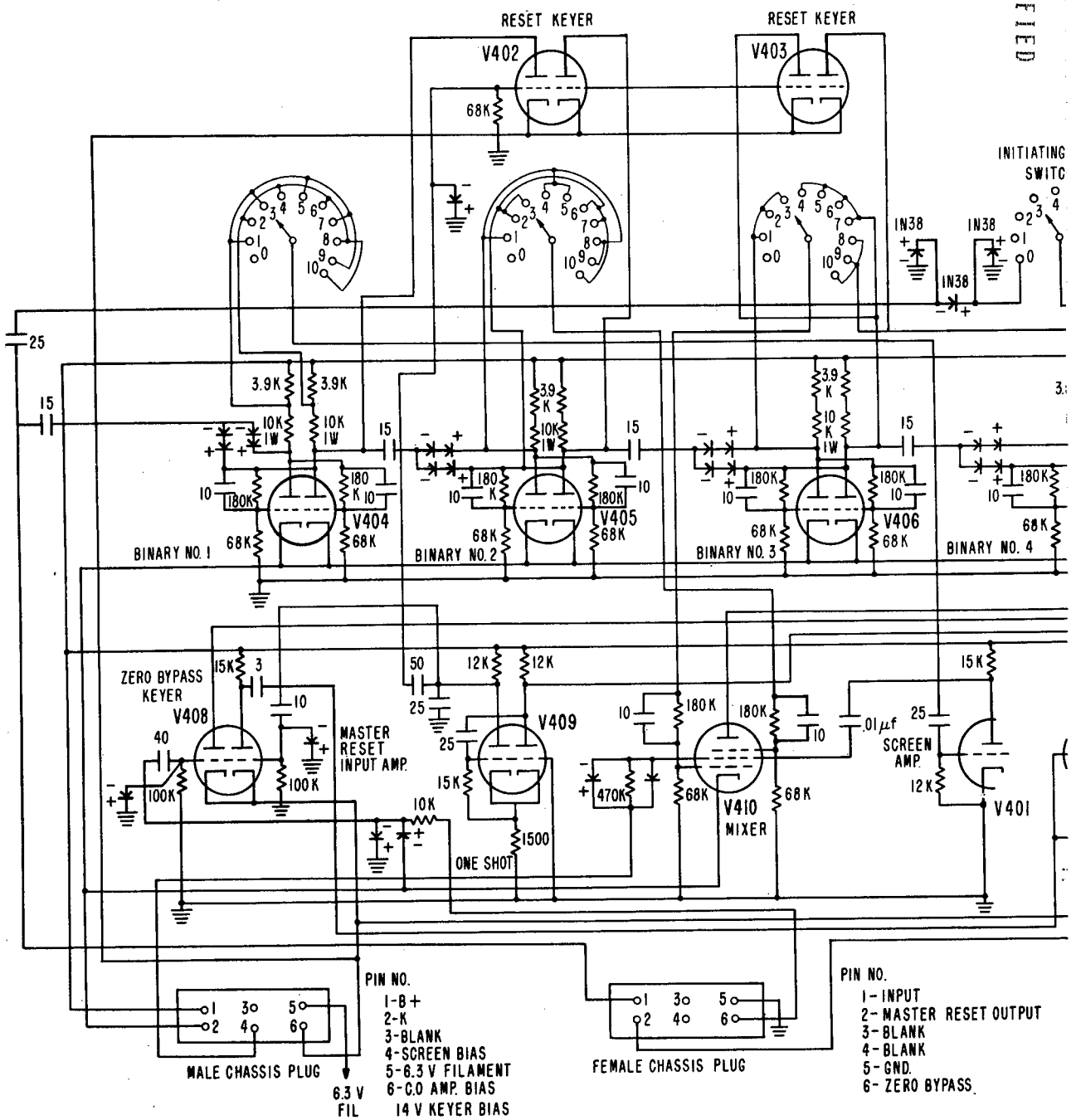


Figure 8 - Schematic diagram of thousands decade

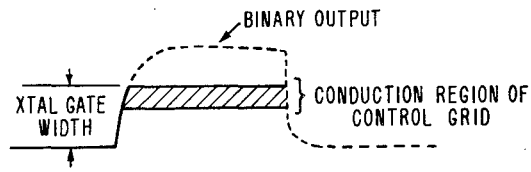


Figure 9 - Delay-amplifier suppressor-grid pulse

Use of the cascaded amplifier in the mixer control grid circuit circumvents a source of trouble encountered when a single amplifier is used. Since reset is made to the output plate of the third binary, the negative pulse at reset will couple from this plate to the positive plate of the fourth binary stage. When reversed through a single amplifier, the negative reset pulse will produce a positive pulse at the mixer control grid. When the pulse occurs, mixer coincidence takes place at a count of one instead of a count of five or nine because of the inherent binary keying delays. Where two cascaded amplifiers are utilized, the first is operated as a normally nonconducting stage and the spurious negative pulse does not affect the amplifier output signal.

The time of the rise and fall for signals at the mixer grids is greatly improved by crystal-diode limiting in both the positive and negative directions. By returning a type-IN34 crystal diode directly to the bias bus, the negative swing is limited at the bias-supply potential and back biasing is thus prevented. The swing in the positive direction is limited by a crystal diode returned from the control grid to the cathode bus and by another from the suppressor grid to the cathode bus. The resulting time of the rise and fall as viewed on either grid is better than 0.1 microsecond (TS 239/UP oscilloscope limitation of response). The mixer screen grid is supplied with a crystal diode to prevent back biasing by returning the screen grid to the bias supply through a crystal diode connected in the necessary polarity direction. By eliminating the back bias the screen may be driven more positive and the mixer output voltage pulse is consequently of greater amplitude.

The selection of binary reference or reset polarities is important in several time respects. Negative reset voltages applied to even-numbered plates 2, 4, 6, and 8 (Table 1) have been shown most suitable for the output-type decade with respect to keying times and simplicity of wiring where direct coupling is used from both second and third wafers to their corresponding mixer grids. The other decades, particularly the input decade, must operate at much higher frequencies so that the time of the pulse rise and fall at the mixer grids must be improved over those of the output decade. Amplifiers and clamping circuits installed between the binaries and the mixer inputs provide a twofold advantage. First, the time of the pulse rise and fall is greatly reduced, and second, by tapping down on the binary plate load resistor, the capacitive load on the binary may be considerably reduced while still retaining sufficient amplifier input voltage. Thus, binary stability is improved. A negative plate is selected from the polarity table to compensate for amplifier inversion. From Table 1 it may be seen that plate 6 would logically be chosen for one of the mixer grid signals for counts 1, 2, and 3. The amplifier circuit, however, is capacitively coupled, and for proper division by these counts, plate 6 remains continually negative and no ac component exists to feed through the coupling condenser. One alternative might be to use direct-coupled amplifiers, but wiring inconvenience and inherent instabilities necessitate that other methods be devised. Reset may be applied to the odd-numbered plates; under these circumstances all binaries will reverse polarity at the first input pulse, and an ac signal will be available for counts 1, 2, and 3. Table 3, however, will show that no selection is available for division by eight except one which produces coincidence prior to the eighth input pulse. Possible selections will either duplicate coincidence conditions for four or seven counts or will duplicate reset polarities. Obviously, preceding counts may not be duplicated, but instability due to duplication of reset polarities is not as apparent. In this case, reset

TABLE 3
Binary Plate Polarity for Odd-Numbered Plate Reset

No. of Input Pulses	P_1 P_2	P_3 P_4	P_5 P_6	P_7 P_8
0 (Reset Ref.)	- +	- +	- +	- +
1	+ -	+ -	+ -	+ -
2	- +	+ -	+ -	+ -
3	+ -	- +	+ -	+ -
4	- +	- +	+ -	+ -
5	+ -	+ -	- +	+ -
6	- +	+ -	- +	+ -
7	+ -	- +	- +	+ -
8	- +	- +	- +	+ -
9	+ -	+ -	+ -	- +
10	- +	+ -	+ -	- +

of the binaries will not cause removal of coincidence signals from the mixer inputs, and consequently the mixer output pulse is determined solely by the width of the differentiated screen-grid pulse. Binary reset, however, follows the time of coincidence by the amount of reset delay and is less than the screen pulsewidth. The reset signal to the first binary is fed back to the mixer screen grid through the differentiating circuit as a second pulse which will augment the original signal, and a step occurs in the mixer output. To avoid operation near this point, care must then be exercised or a reset-time instability occurs. Table 2 uses a combination of odd- and even-plate reset in a manner which provides stable operation on all counts and is considered most suitable for the input-type decades.

The remainder of the circuits in loop No. 1 must also meet certain requirements if all counts are to be satisfactorily obtained throughout the frequency range. The gate must be fully keyed so that loss of the keying signal will not permit the gate to return to the starting condition. To permit stable reset over a wide range of bias voltages, the reset signal at the reset keyer grids must have an amplitude as large as 50 volts. The reset pulse must have a good rise and fall time, i.e., of the order of 0.2 microsecond. The start of this reset must be delayed by a time sufficient to assure full keying of the gate before the binaries are reset and before the mixer grid signals are removed. The reset pulsewidth must be no less than 0.8 microsecond. If it is less when the reset pulse disappears, the third binary reset plate will continue to fall and retrigger the fourth binary to the incorrect starting polarity. The width must not exceed approximately 1.0 microsecond. When added to the delay time, this width determines the response time and the corresponding upper frequency limit of loop No. 1.

The circuits designed to accomplish the preceding functions must operate from a gate output signal that is predominately positive for counts 1 through 9, as well as from input signals predominately negative for counts above ten. To avoid the apparent polarity reversal,

the gate signal is fed through a differentiating circuit to grid key a one-shot multivibrator. The grid contains a crystal diode returned to ground and connected to prevent back biasing. The grid is normally cut off so that only positive spikes from the differentiating circuit will key the multivibrator, and the signal polarity problem is thus eliminated.

The multivibrator provides an output pulse of constant width determined by the cross-coupling time constant and stray capacities. The rise of the output plate is relatively slow. Output of the second one-shot multivibrator plate is fed to the delay amplifier where the delay is introduced in the grid circuit. The amplifier is cut off by a relatively large bias voltage which requires about one-half of the multivibrator output amplitude to cause current conduction. The delay time in reaching this amplitude has been set for the required circuit delay.

The delay-amplifier output is fed to the binary reset amplifier through a unidirectional coupler consisting of three crystal diodes. These are arranged so that only a negative signal may be coupled to the amplifier grid and so that negative signals applied to the same grid through loop No. 2 will not be coupled back to the delay-amplifier plate circuit. This arrangement prevents excessive loading to loop No. 2 and is also used as a gate circuit to prevent base-line feedthrough from reaching the binary reset amplifier grid. Only that part of the negative signal in excess of the 1.5-volts bias will be coupled to that grid circuit.

The binary reset amplifier is zero biased and uses two triodes in parallel to supply the necessary rise time and driving power required in driving the combined capacity loads of the binary reset keyer grid bus and the zero-bypass output cable. The keyer grid bus is coupled to ground through a crystal diode to prevent back biasing that would normally accompany overdrive and add to the keying time. To utilize the maximum bias range, the signal on the grid bus must be free of extraneous signals. Decoupling resistors in the two loads prevent clamping in either load from affecting the other.

Each binary divider requires a keying time of 0.075 microsecond. This time, however, could be considerably reduced by means of crystal clamping in the binary stages, but in this divider the shorter times were not necessary to justify the added complexity. The longest keying time of the mixer will occur on counts 1 and 5 where the change in polarity of the third and fourth binaries are required to fulfill the conditions of mixer coincidence. On count 5, the fourth binary rises in 0.3 microsecond, the mixer delay is about 0.1 microsecond, and the shaper and keyer delays total 0.2 microsecond. The total over-all delay for loop No. 1 is then 0.6 microsecond. If the reset pulsewidth is made 1.0 microsecond, the delay plus pulsewidth becomes 1.6 microseconds, and the top frequency limit of loop No. 1 will be $10^6/1.6$, or 600 kc for this count.

Loop No. 2

The fixed-mixer circuit considerations of loop No. 2 are similar to those of the variable mixer of loop No. 1. This mixer, however, is permanently connected for division by ten; as a result, many of the difficulties found in the design of the variable mixer are not encountered. For example, the third-wafer (control-grid input) delay circuit of the variable mixer is not required since the counts at which delay is essential are not utilized. AC coupling can be used in the control-grid circuit without an amplifier, and mixer keying time will be unaffected since the control grid rises at the fifth input pulse. A connection to the direct plate of the binary is necessary for obtaining sufficient voltage swing; yet resistance decoupling must be used in preventing capacitive loading of the binary plate to avoid unstable operation.

The fixed-circuit one-shot multivibrator must produce, without excessive delay, a pulse that has the correct width and is capable of being fully triggered. In loop No. 2, the one-shot pulsewidth determines the width of the binary reset pulse which at the reset keyer grids

must be about equal in width, rise time, fall time, and amplitude to the pulse produced at that point through loop No. 1. Here, the delay between the one-shot multivibrator and the binary reset grid bus need not be as great as in loop No. 1 since insufficient delay results only in failure of the multivibrator to fully key. As a result, a lower amplitude output is produced by the amplifying action of the multivibrator at a reduced input-signal level. In this case, the multivibrator fails to fully key because its amplified output has been sufficient to reset the binaries through reset loop No. 2, thereby removing the coincident signals from the mixer. It is desirable, of course, that the multivibrator be fully keyed to insure that the removal of the mixer signal has occurred as a result of reset by all binaries and not just one or two.

The delay necessary to assure full keying is obtained in the unidirectional coupler of loop No. 2 and follows the fixed-circuit output amplifier. The input crystal diode of the coupler is returned to the keyer bias bus (approximately 14 volts), thus allowing only that part of negative signals in excess of this bias voltage to feed through to the binary reset amplifier grid. This delay should be 0.2 microsecond or less. The remainder of loop No. 2 coincides with loop No. 1.

The delay in reset through loop No. 2 will include 0.1-microsecond keying time of the first binary (other binaries in coincident polarity prior to first binary keying), 0.2 microsecond at the mixer, 0.2 microsecond for the unidirectional coupler, and 0.1 microsecond for the reset keyer delay. The sum of these delays is 0.6 microsecond, and when this figure is added to a reset pulsewidth of 1.0 microsecond, the total delay is 1.6 microseconds, a figure which corresponds to a top frequency limit of 600 kc.

Loop No. 3

Adequate last-decade binary reset time is not difficult to achieve because division of at least 10:1 will occur in a prior decade so that the available period for binary reset through loop No. 3 is greater by a factor of 10 than for the preceding decade. However, the mixer and the master reset and the one-shot multivibrator are common with loop No. 4, and here it is imperative to minimize reset time. Reset of the binaries, therefore, will occur through loop No. 3 as rapidly as binary reset in other decades.

The mixer circuit is different from those of the units-type decades because the suppressor and control grids are directly coupled from the binary output plates through a network similar to the cross coupling within binaries. Such technique is necessary since this decade must operate at very low frequencies where adequate condensers for ac coupling become excessively large. In addition, even plate reset of the binaries is used, and the polarity table is necessarily different from that of the other type decade. The mixer functions as plate keyer for the multivibrator. To assure full keying by the multivibrator before the binaries are reset, a delay circuit is inserted between the multivibrator and the reset keyer grid bus. The keying times in loop No. 3 are greatest for a count of eight. In this instance, the binary keying delay is 0.3 microsecond, the mixer delay is approximately 0.2 microsecond, the multivibrator delay is 0.2 microsecond, and the reset delay is 0.1 microsecond; the total is 0.8 microsecond. Because of lower input frequencies, the reset pulsewidth is not critical and the reset time is well within operating limits.

Loop No. 4 (Master Reset)

The keying times of loop No. 4 are of prime importance whenever the input decade is set to one. The gate of the input decade must be reset in a time about equal to the time between input pulses of the highest frequency for this count selection. The input pulse which initiated master reset is delayed in each units-type decade by the first binary keying

time, the fixed-circuit mixer delay, the fixed multivibrator delay, and output-amplifier delay. In the output decade, the binary and mixer delays vary with count but the longest will be for a setting of eight. These output-decade delays and the multivibrator keying delay will be added to the master reset time. The delays and pulsewidth in master reset loop No. 4 are also added. The gate keying time through the variable mixer of the input decade is small, but adds to the allowable time in which master reset must occur. This delay may be subtracted from the over-all master reset time delay. All of the preceding times may be summarized as follows:

Master Reset Time Delay

Binary one	0.075 microsecond
Fixed-circuit mixer and multivibrator	0.2
Output amplifier	0.05
	0.3

In a four-decade divider the delay of the units, tens, and hundreds decades would each be as shown above and would total 0.9 microsecond.

Thousands binaries (set to 8)	0.3 microsecond
Thousands mixer	0.2
Thousands multivibrator	0.2
Units-gate keyer	0.1
	0.8

If the units-gate keying delay that tends to decrease the over-all time is neglected, the four-decade reset of the units-decade gate through loop No. 4 is $(3 \times 0.3) + 0.8 = 1.7$ microseconds. The upper frequency limit is then about $10^6/1.7 = 585$ kc.

Loop No. 5

Loop No. 5 is the zero bypass circuit utilized in a multiple-decade divider whenever a decade is set to zero at the same time preceding digits of the division ratio are also zero. This condition occurs when the first significant digit in the division ratio follows the digit of the division ratio corresponding to the decade in question. In a two-decade divider, loop No. 5 is used only when the thousands decade is set for zero. Then the thousands binary and mixer circuits are bypassed; the output of the units decade derived from the binary reset amplifier is fed into the thousands decade just to key the multivibrator and initiate master reset. Sufficiently short reset times are easily obtained because little or no delay is contributed by the essentially bypassed decade. Loop No. 5 coincides with loop No. 1 through the variable gate circuit to the binary reset amplifier where circuit design is dictated by loop No. 1. The return path to the gate of the units decade is made through loop No. 4 which has but slight delay. The only additional component not common with these loops is the thousands-decade multivibrator keyer which has but a slight delay. In loop No. 5 over-all delay time is in no way a limiting factor in upper-frequency response except for division by one, and even at this count, the delay may be made less than that encountered in loop No. 1 for the same division setting.

GENERAL DESIGN CONSIDERATIONS

The preceding discussion shows that a multiplicity of frequencies and wide variation of duty cycles are involved in the design of the four-decade divider. The input frequency and also the setting of division ratio may be varied. The design of the four-decade divider was made to cover a far greater range of application than that required in the proposed frequency meter. In striving for the best stability for the immediate application, the design was directed toward this end, but does not use the full potentialities of this type of four-decade divider. For example, the upper-frequency limit may be increased by some added complexity of the binary circuits; immediate application, however, did not justify such an extension. Also, the use of direct coupling in all decades would permit outputs of extremely low frequencies which would be measured in terms of seconds per cycle and might be useful in establishing accurate time markers. This modification would somewhat limit the high-frequency response and was unjustified by the immediate application.

Where operation is within the limits of the intended application, great care was exercised in other respects to produce circuits that are not sensitive to frequency, duty cycle, and even pulse polarity where required. An attempt was made to permit operation over wide ranges of supply voltages by making circuits self-compensating where possible and carefully avoiding the use of voltage regulation which would increase the instrument size and weight.

The mechanical construction was designed so that all binary dividers are the plug-in type and all are electrically and mechanically identical. The decades, falling into essentially two types, are constructed to plug into a common mounting rack. These features permit servicing by a replacement process without requiring an excessive variety of parts. Tube types have been minimized so that only two varieties, namely the 5670 and 6AS6, are required by the four-decade system.

OPERATION OF THE COMPLETED FOUR-DECADE DIVIDER

Verification of the actual exact division ratio was accomplished by presentation of the divider output together with marker pulses on a TS-239/UP or Dumont 303A oscilloscope. Four groups of these marker pulses, one derived from the input of each decade in the four-decade divider, are superimposed on the output signal and are presented on the scope. To avoid confusion between different groups of markers, each group is adjusted to a different amplitude level. The four-decade-divider output normally has a pulse approximately one-microsecond in width, but this figure is increased by a one-shot multivibrator for convenience in synchronization of the scope trace and for discrimination between the divider output and the marker signals. Before providing one input pulse the units, tens, and hundreds decades count the number of input pulses to that decade, as indicated by the corresponding selector switch, plus an additional group of ten input pulses. One output pulse is obtained, thereafter, for each group of ten input pulses until the over-all selected count is complete. Verification is easily made by examining the scope presentation with the sweep expanded so that the input pulses to the decade in question may be counted. Figures 10 through 13 show a sample scope presentation for a division ratio of 3529. The thousands markers (input to thousands decade) were adjusted for the largest marker amplitude, and the amplitude of the hundreds, tens, and units are decreased in that order. The full division cycle is presented in Figure 11, and three thousands markers are visible with the third corresponding to the start of the next division cycle; hence a thousands-selector-switch setting of 3 is verified. From the same figure, 15 hundreds markers prior to the first thousands marker will be noted, and 10 hundreds markers can also be seen between the next two thousands markers. These observations will verify the accuracy of the 5 setting on the hundreds decade. To expand the space between the tens markers and make counting possible, it is necessary to reduce the sweep time. This decrease is shown in Figure 12; here 12 tens

markers are present in the first group and two additional hundreds markers show 10 tens pulses between each subsequent pair of hundreds markers. Following groups may be viewed by making proper scope adjustments. The scope sweep time must again be decreased to view the units markers (Figure 13). Nineteen units markers which correspond to a setting of 9 are observed prior to the first tens marker. Following tens groups consist of 10 units markers. Thus the over-all division ratio of 3529 was verified by an exact means.

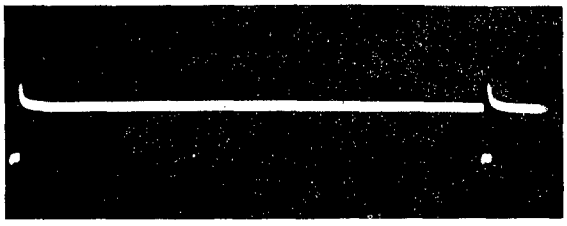


Figure 10 - Scope presentation of divider output for division by 3529

Figure 11 - Divider output with positive marker pulses added

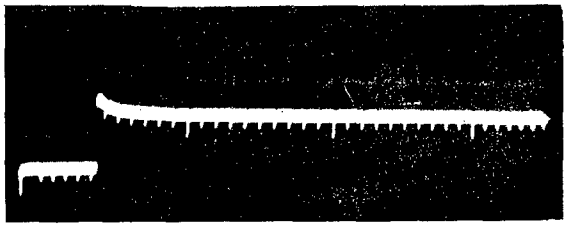


Figure 12 - Divider output with scope sweep expanded to enable a count of tens markers

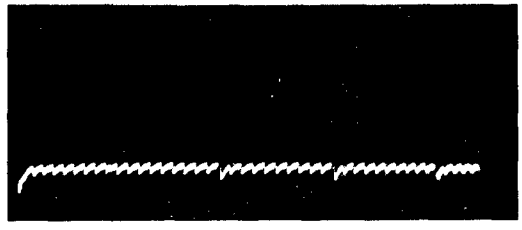


Figure 13 - Divider output with scope sweep further expanded to observe units markers

Once the procedure is established, the counting may be rapidly accomplished. Sweep speeds of the scope may be quickly changed by the switch control. Additionally, after one count has been made, such as the preceding units count of 19, changing the units selector switch will cause the first tens marker to step one pulse for each switch position. In this way, all positions of a decade selector switch may be checked for a single scope adjustment without recounting pulses at each switch setting, and more rapid verification of a large number of division ratios is thereby permitted.

A fantastically large number of possible combinations of input frequencies, division ratios, and operating voltages exists even over the limited frequency range required of the divider for its intended frequency-meter application. A large amount of data was accumulated, but that shown in Tables 4 and 5 is representative of the four-decade-divider operation. In the required measurements, facilities were provided to allow independent variation of each bias voltage of each decade to determine its operating range. In actual use, however, all decades will obtain bias voltages from a common supply which provides only the four required. All bias ranges are wide enough to allow operation of this, a precise frequency divider, without voltage regulation. All bias voltages were made dependent upon supply voltage, and they are self-compensating with supply-voltage variations. Previous data have shown operation over a B+ range of 200 v ± 100. Tables 4 and 5 show that the operating range at a center voltage of 200 is adequate.

TABLE 4
Bias Range Test for 100-Kc Input Frequency

Division Ratio	Bias Conditions	Units Decade Bias Voltages		Tens Decade Bias Voltages		Hundreds Decade Bias Voltages		Thousands Decade Bias Voltages	
		Min.	Max.	Min.	Max.	Min.	Max.	Min.	Max.
3000	K	30	50	35	46	34	51	29	41.5
	Screen	0	36	0	32	12	30.5	0	31
	C. O.	8	24	8	34	10	37	6.5	20
	Gate	0	4.4	0	5	0	6		
3001 - 3009 (Units Control Varied)	K	34	46						
	Screen	20	33						
	C. O.	7	21						
	Gate	0	12						
3001 - 3091 (Tens Control Varied)	K			34.5	44				
	Screen			10	32				
	C. O.			9	16				
	Gate			0	5				
3011 - 3911 (Hundreds Control Varied)	K					37	47		
	Screen					10	33		
	C. O.					10	20.5		
	Gate					0	6		
0111 - 4111 (Thousands Control Varied)	K							30	42
	Screen							0	32
	C. O.							7	19

TABLE 5
Bias Range Test for 350-Kc Input Frequency

Division Ratio	Bias Conditions	Units Decade Bias Voltages		Tens Decade Bias Voltages		Hundreds Decade Bias Voltages		Thousands Decade Bias Voltages	
		Min.	Max.	Min.	Max.	Min.	Max.	Min.	Max.
3521 - 3529 (Units Control Varied)	K	32	41						
	Screen	0	30						
	C. O.	11	24						
	Gate	0	10						
3509 - 3599 (Tens Control Varied)	K			36	41.5				
	Screen			18	30				
	C. O.			16	22				
	Gate			0	8				
3029 - 3929 (Hundreds Control Varied)	K					37	50		
	Screen					5	26.5		
	C. O.					12	24		
	Gate					0	9		
3529 - 10529 (Thousands Control Varied)	K							30	39
	Screen							0	30
	C. O.							8	19

CONCLUSIONS

The circuit research, design, development, and construction of a laboratory model for the direct-reading four-decade frequency divider has been successfully completed. By a selection of four, decade selector switches for input frequencies between the low a-f range and 450 kc, this equipment provides exact and continuous division by any whole number between 1 and 10,999 without any adjustments whatsoever for input frequency. Although the design considerations are complex because of time sequences in operation, feedback loops, frequency range, etc., the problem of reproducing the dividers is not difficult. Components in the four binary dividers of each decade have a one percent tolerance whereas five-percent tolerance is utilized for components of all other circuits. Tube requirements in all but the binary-divider circuits do not require selection beyond meeting JAN requirements. Critical balance in the double-triode binary tubes is not necessary, but extreme unbalance in these tubes will limit binary operation. Only two tube types are required; one is the 6AS6, and the other a choice of the 6J6, 2C51, or 5670. The 6J6, a 7-pin miniature, occupies less chassis-mounting area than the 2C51 or 5670, 9-pin noval basetypes, but thegreater filament-current requirement of the 6J6 makes it less desirable in this respect. To permit servicing by relatively unskilled maintenance men through a substitution method, binary dividers were constructed as plug-in units, and each decade was built on a chassis that plugs into a four-chassis mounting rack. Of the four required decades there are just two basic types, the units and the thousands.

The direct-reading four-decade divider as completed is adequate for the frequency-control device proposed for solving the frequency-meter problem under which the equipment was developed. It should also prove useful for other applications because it is direct reading, is insensitive to input-frequency changes below 450 kc, will divide by any integer from 1 to 10,999 including all prime numbers, and provides instantaneous and simple selection by four ten-position rotary switches.

* * *

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